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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3399.2US (97-629.2)
First Inventor or Application Identifier	Larry D. Kinsman
Title	VERTICALLY MOUNTABLE SEMICONDUCTOR DEVICE AND METHOD
Express Mail Label No.	EL413914405US

09/471,263 12/27/99 U.S. PTO

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 14] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]
4. Oath or Declaration [Total Pages 1]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F R. §§ 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No 09 / 014,503

Prior application information: Examiner J. Clark Group / Art Unit: 2815

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Signature	Brick Power	Date	12/27/1999

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PATENT
Attorney Docket 3399.2US (97-629.2)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL413914405US

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APPLICATION FOR LETTERS PATENT

for

VERTICALLY MOUNTABLE SEMICONDUCTOR DEVICE AND METHODS

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VERTICALLY MOUNTABLE SEMICONDUCTOR DEVICE AND METHODS

BACKGROUND OF THE INVENTION

Cross Reference to Related Application: This application is a continuation of application Serial No. 09/014,053, filed January 27, 1998, pending.

Field of the Invention: The present invention relates to chip-on-board assemblies. Particularly, the present invention relates to vertically mountable, bare or minimally packaged semiconductor devices. The semiconductor devices to which the present invention relates include bond pads proximate an edge thereof. In use, the solder bump establishes an electrical connection with a terminal of a carrier substrate, and supports the semiconductor device perpendicularly relative to the carrier substrate.

Background of Related Art: The direct attachment of a semiconductor device to a circuit board is known in the art as chip-on-board technology. Semiconductor devices that are directly mountable to a circuit board typically include bond pads along more than one edge thereof or in an area array over the active surface thereof. Methods for attaching semiconductor devices directly to a circuit board include flip-chip technology and tape automated bonding. Typically, when those techniques are employed, a semiconductor device is oriented over the circuit board and substantially parallel thereto in order to establish an electrical connection between the semiconductor device and the circuit board. After connecting such a semiconductor device to a circuit board, a protective coating may be applied over the semiconductor device.

However, the placement of a semiconductor device directly against a circuit board is somewhat undesirable in that, due to the parallel orientation of the semiconductor device relative to the circuit board and the typical placement of the semiconductor device's active surface thereagainst, heat must pass through both the circuit board and the semiconductor device in order to dissipate from the semiconductor device. Thus, the transfer of heat away from the semiconductor device is relatively slow. The horizontal orientation of the semiconductor device also consumes a great deal of "real estate" or area on the circuit board.

Vertical surface mount packages are also known in the art. When compared with traditional, horizontally mountable semiconductor packages and chip-on-board semiconductor devices, many vertical surface mount packages have a superior ability to transfer heat away from the semiconductor device. Vertical surface mount packages also consume less area on a circuit board than a horizontally mounted package of the same size. Thus, many skilled individuals in the semiconductor industry are finding vertical surface mount packages more desirable than their traditional, horizontally mountable counterparts and horizontally mountable chip-on-board devices.

The following United States Patents disclose various exemplary vertical surface mount packages: Re. 34,794, issued to Warren M. Farnworth on November 22, 1994; 5,444,304, issued to Kouija Hara and Jun Tanabe on August 22, 1995; 5,450,289, issued to Yooung D. Kweon and Min C. An on September 12, 1995; 5,451,815, issued to Norio Taniguchi et al. on September 19, 1995; 5,592,019, issued to Tetsuya Ueda et al. on January 7, 1997; and 5,635,760, issued to Toru Ishikawa on June 3, 1997.

Many vertical surface mount packages in the prior art are somewhat undesirable in that they include leads which operatively connect a semiconductor device to a circuit board. The leads of such devices tend to increase the impedance and decrease the overall speed with which a device conducts electrical signals. Moreover, the packaging of many such devices adds to their undesirability. Typically, packaging requires multiple additional manufacturing steps, which translates into increased production costs. The packaging of many vertical surface mount packages also tends to consume a substantial amount of space on the circuit board.

United States Patent 5,668,409 (the "'409 patent"), issued to Stephen Joseph Gaul on September 16, 1997, discloses a vertically mountable, bare semiconductor die which includes bond pads along the edge thereof. The '409 patent discloses vertical mounting of that device to a circuit board by solder reflow techniques. However, that device is somewhat undesirable in that fabrication thereof requires several additional steps relative to the fabrication of typical chip-on-board semiconductor devices. The requirement of

additional fabrication steps, and the related requirement of additional fabrication materials, increases the manufacturing cost of such semiconductor devices.

Thus, a vertically mountable bare semiconductor device is needed which has reduced impedance relative to devices in the prior art, has good thermal conductivity, and consumes less space on a circuit board. A method of mounting a bare or minimally packaged semiconductor device perpendicularly relative to a circuit board is also needed.

SUMMARY OF THE INVENTION

The semiconductor device of the present invention includes bond pads disposed proximate a single edge thereof. Placement of the bond pads proximate an edge of the semiconductor device facilitates direct vertical mounting of the semiconductor device to a carrier substrate. Thus, when such a semiconductor device is substantially perpendicularly mounted to a carrier substrate, packaging and leads are not necessary to establish an electrical connection between the bond pads and the corresponding terminals on the carrier substrate. The direct connection between the bond pads and substrate board contacts also imparts to the semiconductor device assembly of the present invention a low impedance characteristic.

A preferred mounting method according to the present invention includes the placement of a brick of solder paste on the carrier substrate terminals, orienting the semiconductor device perpendicularly relative to the carrier substrate, aligning the bond pads of the semiconductor device with their corresponding terminals, establishing contact between the bumps and the solder paste, and heating the bumps and solder paste to re-flow the solder and attach the bond pads to their respective terminals.

Other advantages of the present invention will become apparent through a consideration of the appended drawings and the ensuing description.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a frontal perspective view of a first embodiment of a semiconductor device-carrier substrate assembly according to the present invention;

Figure 2 is a front plan view of a first embodiment of a semiconductor device for use in the present invention;

Figure 3a is a side plan view of the semiconductor device of Figure 2, illustrating placement of the semiconductor device on a carrier substrate;

Figure 3b is a side plan view of the semiconductor device of Figure 2, illustrating a first preferred attachment of the semiconductor device to the carrier substrate;

Figure 4a is a side plan view of the semiconductor device of Figure 2, illustrating an alternative embodiment of a support member between the semiconductor device and the carrier substrate;

Figure 4b is a side plan view of the semiconductor device of Figure 2, illustrating an alternative embodiment of a support member between the semiconductor device and the carrier substrate;

Figure 5a is a side plan view of a series of laminated semiconductor devices;

Figure 5b is a side plan view of an alternative embodiment of a series of laminated semiconductor devices; and

Figure 6 is a schematic representation of the present invention in a computer.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates a semiconductor device 10 which has been vertically mounted to a carrier substrate 30. Solder joints 20a, 20b, 20c, etc. support semiconductor device 10 relative to carrier substrate 30.

Referring to Figure 2, semiconductor device 10 is a semiconductor device of the type known and used in the industry, which includes circuit traces and active elements. The bond pads 12a, 12b, 12c, etc. of semiconductor device 10 are disposed on active surface 11, adjacent to a single edge 16 of the semiconductor device. Preferably, bond pads 12a, 12b, 12c, etc. are arranged in-line. Bond pads 12a, 12b, 12c, etc. may be

disposed a short distance from edge 16, or their lower edges may be flush with the edge. Thus, during fabrication of semiconductor device 10, bond pads 12a, 12b, 12c, etc. are redirected to a location which is adjacent to edge 16. Methods and mechanisms which are known to those of ordinary skill in the art are useful for manufacturing semiconductor devices which are useful in the package according to the present invention. Such methods include the formation of electrical traces which lead to edge 16 and the fabrication of bond pads 12a, 12b, 12c, etc. adjacent to edge 16. Preferably, the fabrication steps which precede the formation of the electrical traces that lead to bond pads 12a, 12b, 12c, etc. and the formation of the bond pads are unchanged from their equivalent steps in the fabrication of prior art semiconductor devices. Thus, existing semiconductor device designs are useful in the package of the present invention with little modification and no increase in the number of fabrication steps.

A first semiconductor device 10 has a standardized number of bond pads 12a, 12b, 12c, etc., which are spaced apart from one another at a standardized pitch, and which may be positioned at a specific location relative to a center line 18 of the semiconductor device, or relative to any other landmark on the semiconductor device, such as a side thereof. Alternatively, semiconductor device 10 may include a non-standardized number and lateral spacing of bond pads 12. The placement of bond pads 12a, 12b, 12c, etc. proximal to edge 16 imparts semiconductor device 10 with reduced impedance as the bond pads are electrically connected to the carrier substrate (reference character 30 of Figure 1), relative to many vertical surface mount packages and other packaged semiconductor devices in the prior art.

Preferably, bond pads 12a, 12b, 12c, etc. each include a bump 14a, 14b, 14c, etc. formed thereon. Bumps 14a, 14b, 14c, etc. are preferably formed from gold, gold alloy, or solder by techniques which are known in the art.

With reference to Figure 3a, a brick of solder paste 34 is disposed on each terminal 32 of carrier substrate 30. Typically, solder paste 34 is a mixture of solder powder, flux and a binder which keeps the solder powder and flux together. The preferred solder paste 34 and bump 14 materials have matched impedance to ensure

optimum conditions for the transfer of electrical signals from carrier substrate 30 to semiconductor device 10 and from the semiconductor device to the carrier substrate. Preferably, solder paste 34 is applied to terminals 32 by techniques which are known in the art, including without limitation, screen printing, stencil printing, pressure dispensing, and the use of solder preforms.

As semiconductor device 10 is positioned on carrier substrate 30, bump 14 contacts solder paste 34. Bump 14 and solder paste 34 are fused together to form a solder joint 20, which is also referred to as an electrically conductive joint. Solder joint 20 physically supports semiconductor device 10 relative to carrier substrate 30 in substantially a vertical orientation with respect thereto, and electrically connects bond pads 12 to their corresponding terminals 32. Preferably, known solder reflow techniques are employed to form solder joint 20. Solder reflow techniques include, but are not limited to, vapor-phase, infrared, hot gas, and other reflow methods. Other known soldering techniques are also useful for fusing bump 14 and solder paste 34 to electrically connect bond pad 12 to terminal 32. Alternatively, an electrically conductive joint 20 may be formed by placing a connector of electrically conductive epoxy or any other conductive element, including without limitation electrically conductive epoxies and z-axis elastomers, in contact with both bond pad 12 and terminal 32.

Referring now to Figure 4a, one or more support joints 40, which are also referred to as support footings or support members, may be placed between surface 15 of semiconductor device 10 and carrier substrate 30 (i.e., on the side of the semiconductor device opposite electrically conductive joint 20) to impart additional structural stability to the semiconductor device by stabilizing it from both sides. Preferably, support joint 40 is formed from materials such as epoxy potting compounds, acrylic compounds, silicone materials, resinous molding compounds, or other polymeric plastic materials which are known in the art. Preferably, the amount of material used to form support joint 40 is sufficient to support semiconductor device 10, yet minimal in order to optimize the transfer of heat away from the semiconductor device and preserve surface area on the carrier substrate.

Referring to Figure 4b, alternatively or in combination with support joint 40, semiconductor device 10 may include a support layer 42, which is also referred to as a support member, on at least a portion of surface 15. Support layer 42 imparts additional structural support to semiconductor device 10. The materials which are useful for forming support joint 40 are also useful for forming support layer 42. Support layer 42 may be applied to surface 15 by techniques which are known in the art, including without limitation, lamination and adhesive bonding. Alternatively, support layer 42 may be manufactured from materials having good thermal conductivity, such as copper, aluminum, other metals, metal alloys, and ceramics.

Figures 5a and 5b illustrate a laminated module 50 which includes a plurality of adjacent semiconductor devices 10 that is bonded together with a layer of laminate 52. When mounted to carrier substrate 30, laminated module 50 has greater structural stability than a vertically mounted semiconductor device such as that illustrated in Figure 1. Laminate 52 may be formed from the same types of materials that are useful as support layer 42, described above in reference to Figure 4b. Preferably, laminate 52 is manufactured from a material which is a good thermal conductor. Thus, during operation of each semiconductor device 10, laminate 52 facilitates the transfer of heat away from the semiconductor devices attached thereto.

The laminates 52 and 52′ of Figures 5a and 5b, respectively, have different thicknesses. Thinner laminates 52′ are preferred from the standpoint that the number of semiconductor devices 10 that are attachable to a given area of the carrier substrate 30 is maximized as the thickness of the laminate layer is minimized.

Figure 6 illustrates a computer 60 including a circuit board 62. Semiconductor device 10 and laminate module 50 are attached to circuit board 62 in a manner which establishes an electronic connection between the semiconductor devices and the circuit board. Thus, with the attachment of semiconductor device 10 and/or laminate module 50 to circuit board 62, the semiconductor device and/or module is operatively associated with computer 60.

Advantageously, the bond pads of the semiconductor device, which are disposed adjacent an edge thereof, may be directly connected to corresponding terminals on a carrier substrate. Thus, the additional impedance that is typically generated by package leads is significantly reduced. The placement of bond pads on the semiconductor device also facilitates the substantial vertical mounting arrangement of the semiconductor device to a carrier substrate, which, when combined with a convection-type air circulation system, facilitates heat transfer away from the semiconductor device. Preferably, the semiconductor device is bare or minimally packaged, reducing the space consumption thereof relative to vertical surface mount packages and horizontally mountable semiconductor devices and packages. Further, fabrication of the device requires no additional steps relative to the fabrication of many similar semiconductor devices in the prior art. The assembly method of the present invention orients the semiconductor device perpendicularly relative to the carrier substrate.

Although the foregoing description contains many specificities, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention, indicated by the appended claims and their equivalents.

CLAIMS

What is claimed is:

1. A vertical surface mount semiconductor device, comprising:

a semiconductor device;

a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof; and

conductive bumps disposed adjacent selected bond pads, each of said conductive bumps configured to form a conductive joint between one of said selected bond pads and a corresponding terminal of a substrate upon positioning said semiconductor device substantially vertically relative to said substrate.

2. The vertical surface mount semiconductor device of claim 1, wherein a conductive bum is disposed adjacent each of said plurality of bond pads.

3. The vertical surface mount semiconductor device of claim 1, further comprising a support layer.

4. The vertical surface mount semiconductor device of claim 3, wherein said support layer is disposed on another surface of said semiconductor device.

5. The vertical surface mount semiconductor device of claim 1, further comprising a support footing formed adjacent said edge.

6. The vertical surface mount semiconductor device of claim 5, wherein said support footing is disposed on another surface of said semiconductor device.

7. The vertical surface mount semiconductor device of claim 5, wherein said support footing is disposed on said surface of said semiconductor device.

8. The vertical surface mount semiconductor device of claim 1, further comprising a laminate which connectively bonds said semiconductor device to an adjacent semiconductor device.

9. A vertical surface mount semiconductor device, comprising:

a semiconductor device;

a plurality of bond pads disposed on a surface of said semiconductor device adjacent an edge thereof, selected bond pads of said plurality of bond pads having conductive bumps adjacent thereto, said conductive bumps configured to form a joints between said selected bond pads and corresponding terminals of a carrier substrate upon substantially perpendicular orientation of said semiconductor device on said carrier substrate; and

a support member, at least a portion of which is disposed proximate said edge of said semiconductor device.

10. The vertical surface mount semiconductor device of claim 9, wherein said support member is selected from the group consisting of support footings and support layers.

11. The vertical surface mount semiconductor device of claim 9, wherein said support member is disposed on another surface of said semiconductor device.

12. The vertical surface mount semiconductor device of claim 9, wherein a conductive bump is positioned adjacent each of said plurality of bond pads.

13. A chip-on-board assembly, comprising:

a substrate with a plurality of terminals;

a semiconductor device configured to be positioned substantially perpendicularly relative to said substrate, said semiconductor device having a plurality of bond pads on a

surface thereof, each of said plurality of bond pads being located adjacent an edge of said surface; and

electrically conductive joints configured to be disposed and to establish communication between selected bond pads and corresponding terminals.

14. The chip-on-board assembly of claim 13, wherein each of said plurality of bond pads has an electrically conductive joint disposed adjacent thereto.

15. The chip-on-board assembly of claim 13, further comprising a support member in contact with at least one of said semiconductor device and said carrier substrate.

16. The chip-on-board assembly of claim 15, wherein said support member is selected from the group consisting of support footings and support layers.

17. The chip-on-board assembly of claim 15, wherein said support member is disposed proximate said edge of said semiconductor device.

18. The chip-on-board assembly of claim 13, wherein said semiconductor device is laminated to an adjacent semiconductor device.

19. A computer including a vertically mountable semiconductor device, the semiconductor device comprising:

a semiconductor die with a plurality of circuit traces;

a plurality of bond pads disposed on a surface of said semiconductor die proximate an edge thereof, each of said plurality of bond pads communicating with one of said plurality of circuit traces; and

conductive bumps in communication with selected bond pads, said conductive bumps each configured to form a joint between one of said selected bond pads and a

corresponding terminal of a substrate when said semiconductor device is positioned substantially perpendicularly relative to said substrate.

20. The computer of claim 19, wherein each of said plurality of bond pads has a conductive bump in communication therewith.

21. The computer of claim 19, wherein said semiconductor device further comprises a support member.

22. The computer of claim 21, wherein said support member is selected from the group consisting of support footings and support layers.

23. The computer of claim 21, wherein said support member is disposed proximate said edge.

24. The computer of claim 19, wherein said semiconductor device is laminated to an adjacent semiconductor device.

ABSTRACT OF THE DISCLOSURE

A vertically mountable semiconductor device including a plurality of bond pads disposed proximate to a single edge thereof. The bond pads are bumped with an electrically conductive material. The semiconductor device may also include a support member. Alternatively, the semiconductor device may be laminated to one or more adjacent semiconductor devices. The present invention also includes a method of attaching the semiconductor device to a carrier substrate. Preferably, solder paste is applied to terminals on the carrier substrate. The semiconductor device is oriented vertically over the carrier substrate, such that the bumped bond pads align with their corresponding terminals. The bumps are placed into contact with the solder paste. The bumps and solder paste are then fused to form a joint between each of the bond pads and its respective terminal, establishing an electrically conductive connection therebetween and imparting structural stability to the semiconductor device.

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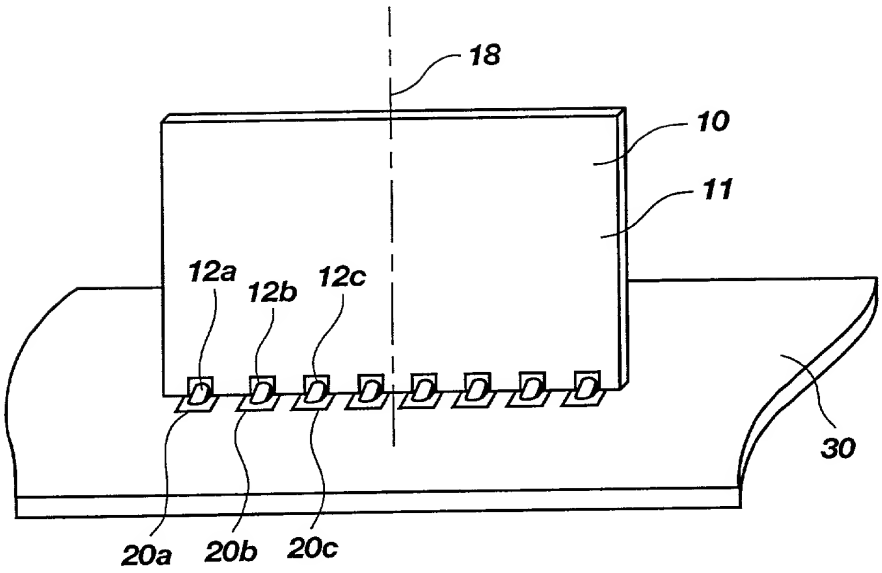

Fig. 1

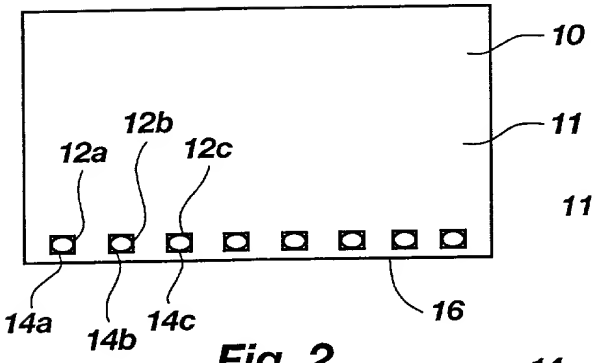

Fig. 2

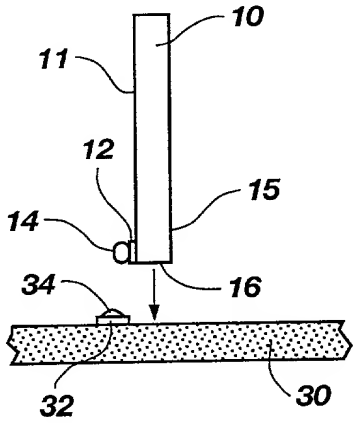

Fig. 3a

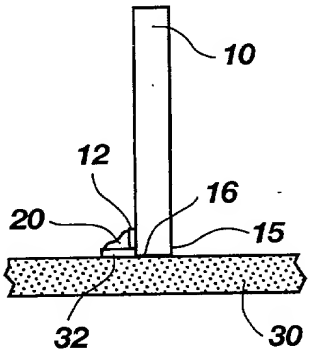

Fig. 3b

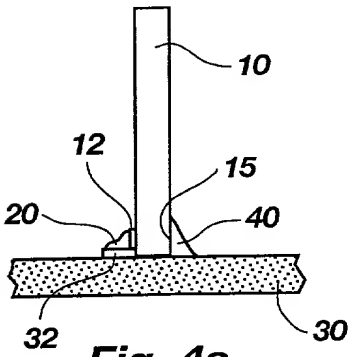

Fig. 4a

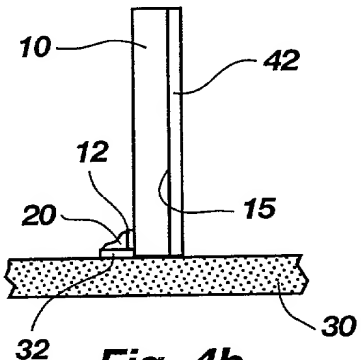

Fig. 4b

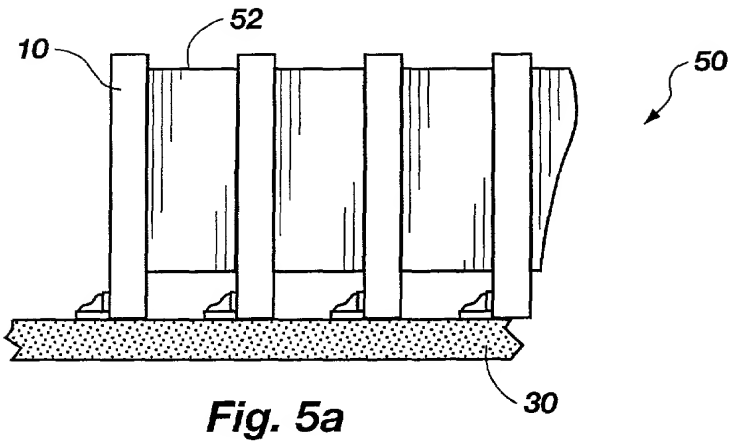

Fig. 5a

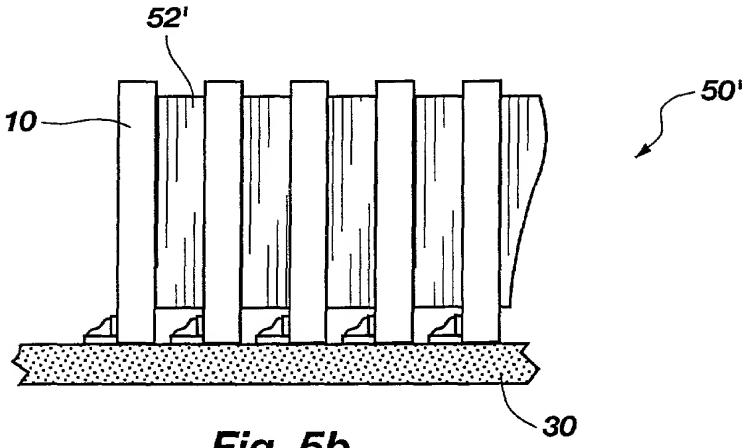

Fig. 5b

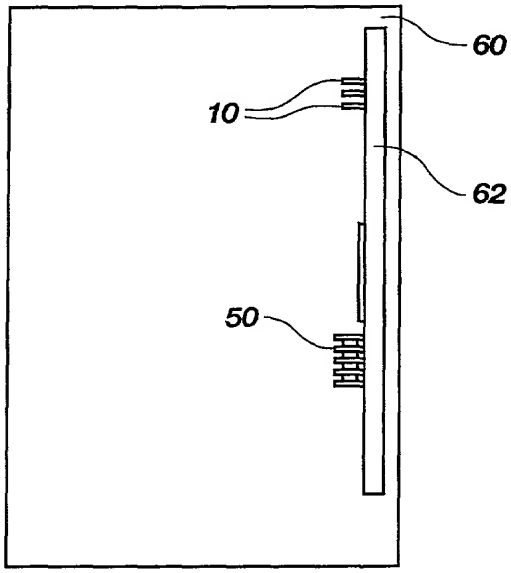

Fig. 6

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled VERTICALLY MOUNTABLE SEMICONDUCTOR DEVICE AND METHODS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
(provisional application no.)	(filing date)
(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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